

# PHB100N03LT

N-channel enhancement mode field-effect transistor

Rev. 01 — 07 September 2000

Product specification

## 1. Description

N-channel enhancement mode field-effect transistor in a plastic package using TrenchMOS™<sup>1</sup> technology.

Product availability:

PHB100N03LT in SOT404 (D<sup>2</sup>-PAK).

## 2. Features

- TrenchMOS™ technology
- Low on-state resistance
- Avalanche ruggedness rated
- Logic level compatible
- Surface mount package.

## 3. Applications

- DC to DC converters
- Synchronous rectification.

## 4. Pinning information

Table 1: Pinning - SOT404, simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1	gate (g)	<p style="text-align: center;">SOT404 (D<sup>2</sup>-PAK)</p>	
2	drain (d) <span style="color: red;">[1]</span>		
3	source (s)		
mb	connected to drain (d)		

[1] It is not possible to make connection to pin 2 of the SOT404 package.

1. TrenchMOS is a trademark of Royal Philips Electronics.



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## 5. Quick reference data

Table 2: Quick reference data

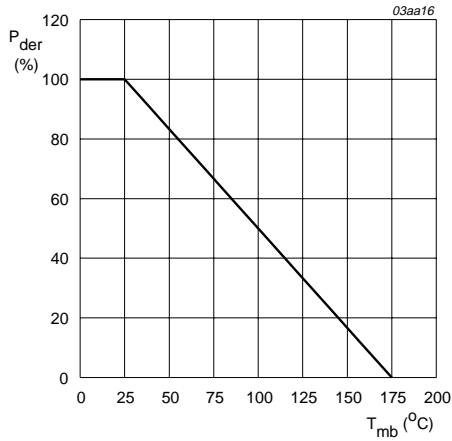
Symbol	Parameter	Conditions	Typ	Max	Unit
$V_{DS}$	drain-source voltage (DC)	$T_j = 25$ to $175$ °C	–	25	V
$I_D$	drain current (DC)	$T_{mb} = 25$ °C; $V_{GS} = 5$ V	–	75	A
$P_{tot}$	total power dissipation	$T_{mb} = 25$ °C	–	125	W
$T_j$	junction temperature		–	175	°C
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10$ V; $I_D = 25$ A	5.0	5.8	mΩ
		$V_{GS} = 5$ V; $I_D = 25$ A	6.2	7.5	mΩ

## 6. Limiting values

Table 3: Limiting values

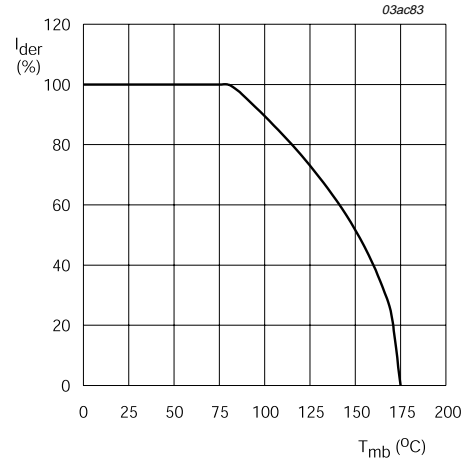
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage (DC)	$T_j = 25$ to $175$ °C	–	25	V
$V_{DGR}$	drain-gate voltage (DC)	$T_j = 25$ to $175$ °C; $R_{GS} = 20$ kΩ	–	25	V
$V_{GS}$	gate-source voltage (DC)		–	±15	V
$V_{GSM}$	peak gate-source voltage	$t_p \leq 50$ μs; pulsed; duty cycle = 25%	–	±20	V
$I_D$	drain current (DC)	$T_{mb} = 25$ °C; $V_{GS} = 5$ V; Figure 2 and 3	–	75	A
		$T_{mb} = 100$ °C; $V_{GS} = 5$ V; Figure 2	–	67	A
$I_{DM}$	peak drain current	$T_{mb} = 25$ °C; pulsed; $t_p \leq 10$ μs; Figure 3	–	240	A
$P_{tot}$	total power dissipation	$T_{mb} = 25$ °C; Figure 1	–	125	W
$T_{stg}$	storage temperature		–55	+175	°C
$T_j$	operating junction temperature		–55	+175	°C
<b>Source-drain diode</b>					
$I_S$	source (diode forward) current (DC)	$T_{mb} = 25$ °C	–	75	A
$I_{SM}$	peak source (diode forward) current	$T_{mb} = 25$ °C; pulsed; $t_p \leq 10$ μs	–	240	A
<b>Avalanche ruggedness</b>					
$E_{AS}$	non-repetitive avalanche energy	unclamped inductive load; $I_D = 75$ A; $t_p = 0.2$ ms; $V_{DD} \leq 15$ V; $R_{GS} = 50$ Ω; $V_{GS} = 5$ V; starting $T_j = 25$ °C; Figure 4	–	240	mJ
$I_{AS}$	non-repetitive avalanche current	unclamped inductive load; $V_{DD} \leq 15$ V; $R_{GS} = 50$ Ω; $V_{GS} = 5$ V; Figure 4	–	75	A



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

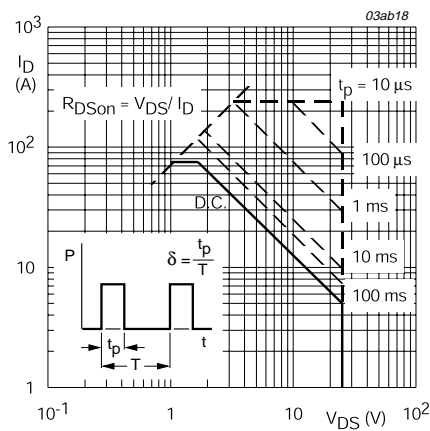
Fig 1. Normalized total power dissipation as a function of mounting base temperature.



V<sub>GS</sub> ≥ 5 V

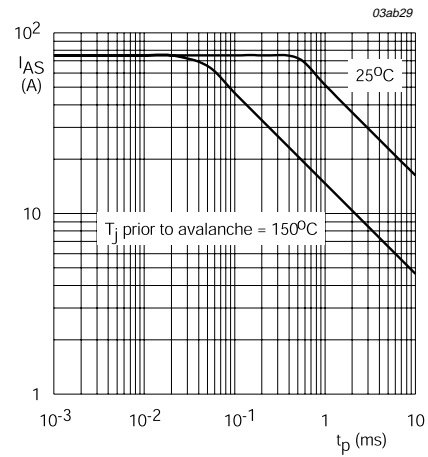
$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of mounting base temperature.



T<sub>mb</sub> = 25 °C; I<sub>DM</sub> is single pulse.

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.



Unclamped inductive load; V<sub>DD</sub> ≤ 15 V; R<sub>GS</sub> = 50 Ω; V<sub>GS</sub> = 5 V; starting T<sub>j</sub> = 25 °C and 150°C.

Fig 4. Non-repetitive avalanche ruggedness current as a function of pulse duration.

## 7. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Value	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Figure 5	1.2	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	mounted on a printed circuit board; minimum footprint	50	K/W

### 7.1 Transient thermal impedance

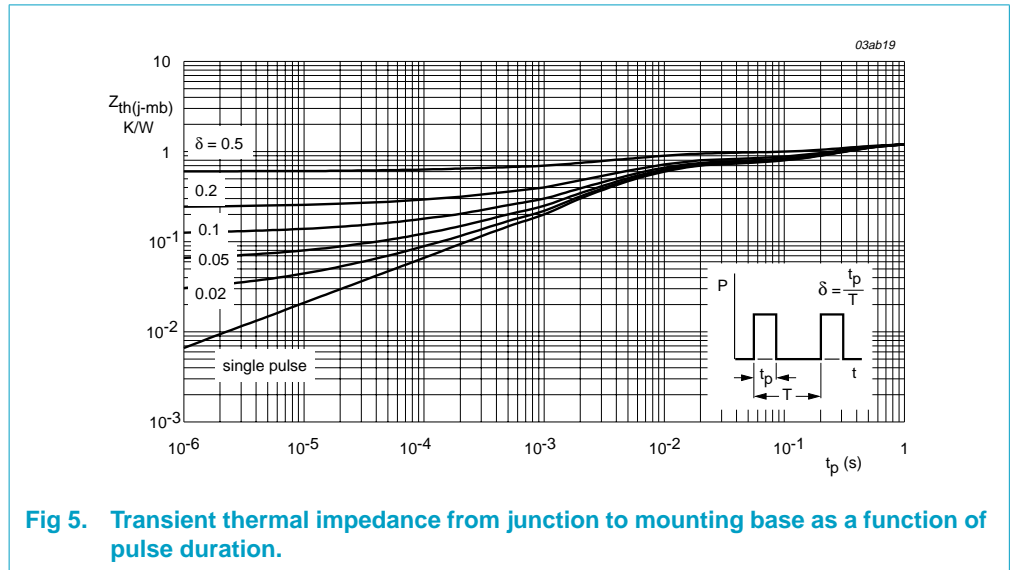
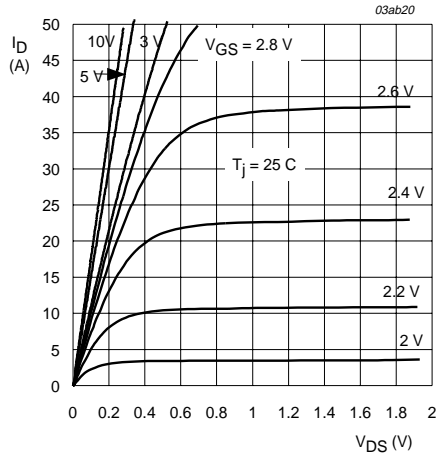


Fig 5. Transient thermal impedance from junction to mounting base as a function of pulse duration.

## 8. Characteristics

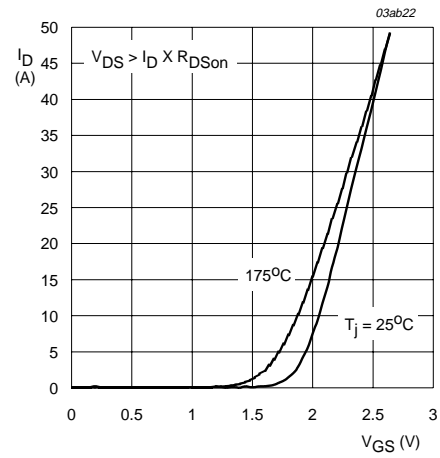
**Table 5: Characteristics**
 $T_j = 25\text{ }^\circ\text{C}$  unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
<b>Static characteristics</b>							
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\ \mu\text{A}$ ; $V_{GS} = 0\ \text{V}$					
		$T_j = 25\text{ }^\circ\text{C}$	25	35	–	V	
		$T_j = -55\text{ }^\circ\text{C}$	23	–	–	V	
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\ \text{mA}$ ; $V_{DS} = V_{GS}$ ; Figure 10					
		$T_j = 25\text{ }^\circ\text{C}$	1	1.5	2	V	
		$T_j = 175\text{ }^\circ\text{C}$	0.5	–	–	V	
		$T_j = -55\text{ }^\circ\text{C}$	–	–	2.3	V	
$I_{DSS}$	drain-source leakage current	$V_{DS} = 25\ \text{V}$ ; $V_{GS} = 0\ \text{V}$					
		$T_j = 25\text{ }^\circ\text{C}$	–	0.05	10	$\mu\text{A}$	
		$T_j = 175\text{ }^\circ\text{C}$	–	5.0	500	$\mu\text{A}$	
$I_{GSS}$	gate-source leakage current	$V_{GS} = \pm 10\ \text{V}$ ; $V_{DS} = 0\ \text{V}$	–	10	100	nA	
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\ \text{V}$ ; $I_D = 25\ \text{A}$ ; Figure 8 and 9					
		$T_j = 25\text{ }^\circ\text{C}$	–	5	5.8	m $\Omega$	
		$V_{GS} = 5\ \text{V}$ ; $I_D = 25\ \text{A}$ ; Figure 8 and 9					
		$T_j = 25\text{ }^\circ\text{C}$	–	6.2	7.5	m $\Omega$	
		$T_j = 175\text{ }^\circ\text{C}$	–	–	14	m $\Omega$	
<b>Dynamic characteristics</b>							
$g_{fs}$	forward transconductance	$V_{DS} = 25\ \text{V}$ ; $I_D = 25\ \text{A}$ ; Figure 12	–	68	–	S	
$Q_{g(tot)}$	total gate charge	$I_D = 75\ \text{A}$ ; $V_{DS} = 15\ \text{V}$ ; $V_{GS} = 5\ \text{V}$ ; Figure 15	–	60	–	nC	
$Q_{gs}$	gate-source charge		–	8	–	nC	
$Q_{gd}$	gate-drain (Miller) charge		–	32	–	nC	
$C_{iss}$	input capacitance	$V_{GS} = 0\ \text{V}$ ; $V_{DS} = 25\ \text{V}$ ; $f = 1\ \text{MHz}$ ; Figure 13	–	3500	–	pF	
$C_{oss}$	output capacitance		–	970	–	pF	
$C_{rss}$	reverse transfer capacitance		–	640	–	pF	
$t_{d(on)}$	turn-on delay time	$V_{DD} = 15\ \text{V}$ ; $R_D = 0.6\ \Omega$ ;	–	21	–	ns	
$t_r$	turn-off rise time	$V_{GS} = 5\ \text{V}$ ; $R_G = 10\ \Omega$	–	170	–	ns	
$t_{d(off)}$	turn-off delay time		–	270	–	ns	
$t_f$	turn-off fall time		–	216	–	ns	
<b>Source-drain diode</b>							
$V_{SD}$	source-drain (diode forward) voltage	$I_S = 25\ \text{A}$ ; $V_{GS} = 0\ \text{V}$ ; Figure 14	–	0.95	1.2	V	
$t_{rr}$	reverse recovery time	$I_S = 25\ \text{A}$ ;	–	140	–	ns	
$Q_r$	recovered charge	$di_S/dt = -100\ \text{A}/\mu\text{s}$ ; $V_{GS} = 0\ \text{V}$ ; $V_{DS} = 25\ \text{V}$	–	270	–	nC	



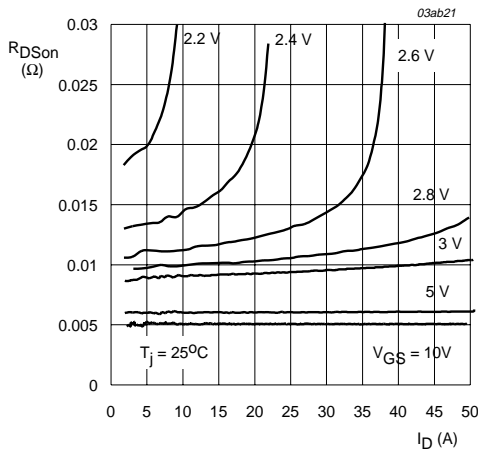
$T_j = 25\text{ }^\circ\text{C}$

**Fig 6. Output characteristics: drain current as a function of drain-source voltage; typical values.**



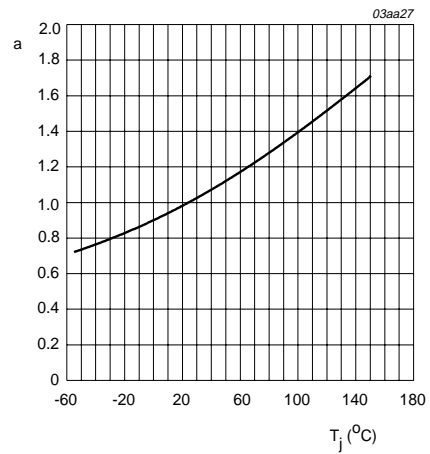
$T_j = 25\text{ }^\circ\text{C}$  and  $175\text{ }^\circ\text{C}$ ;  $V_{DS} > I_D \times R_{DSon}$

**Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values.**



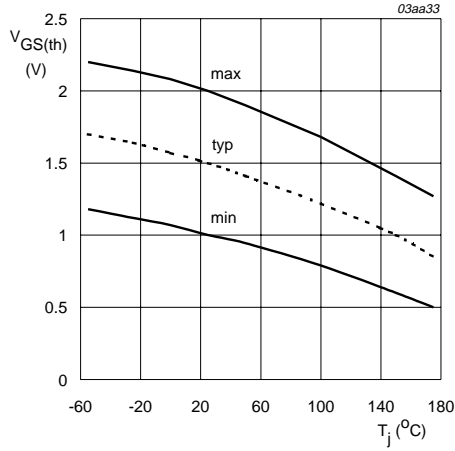
$T_j = 25\text{ }^\circ\text{C}$

**Fig 8. Drain-source on-state resistance as a function of drain current; typical values.**



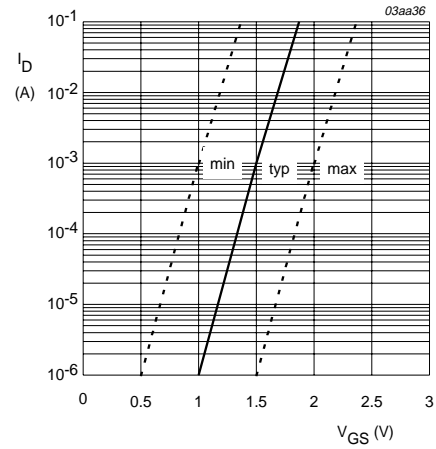
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

**Fig 9. Normalized drain-source on-state resistance factor as a function of junction temperature.**



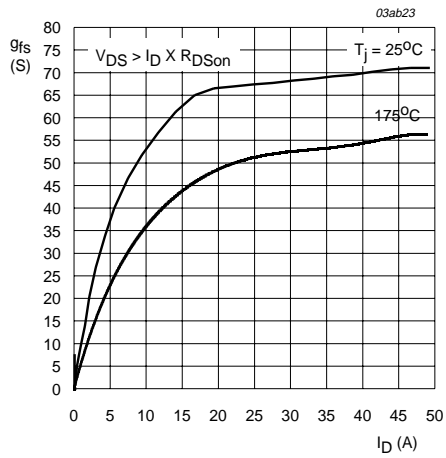
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

**Fig 10. Gate-source threshold voltage as a function of junction temperature.**



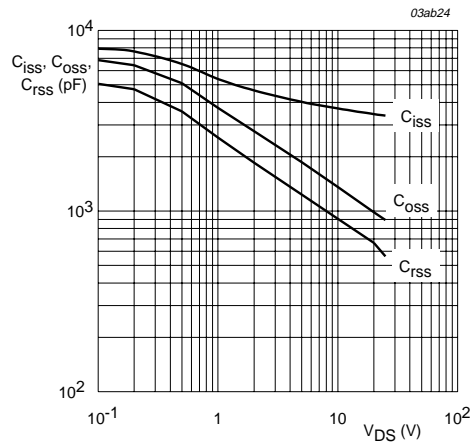
$T_j = 25 \text{ }^{\circ}C; V_{DS} = 5 \text{ V}$

**Fig 11. Sub-threshold drain current as a function of gate-source voltage.**



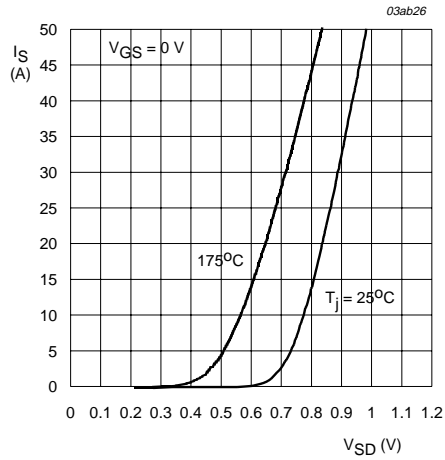
$T_j = 25 \text{ }^{\circ}C$  and  $175 \text{ }^{\circ}C; V_{DS} > I_D \times R_{DS(on)}$

**Fig 12. Forward transconductance as a function of drain current; typical values.**



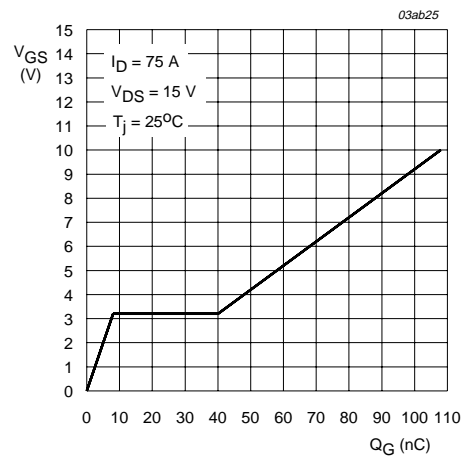
$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

**Fig 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.**



$T_j = 25^\circ\text{C}$  and  $175^\circ\text{C}$ ;  $V_{GS} = 0\text{ V}$

**Fig 14. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.**



$I_D = 75\text{ A}$ ;  $V_{DS} = 15\text{ V}$

**Fig 15. Gate-source voltage as a function of gate charge; typical values.**



9. Package outline

Plastic single-ended surface mounted package (Philips version of D<sup>2</sup>-PAK); 3 leads  
(one lead cropped)

SOT404

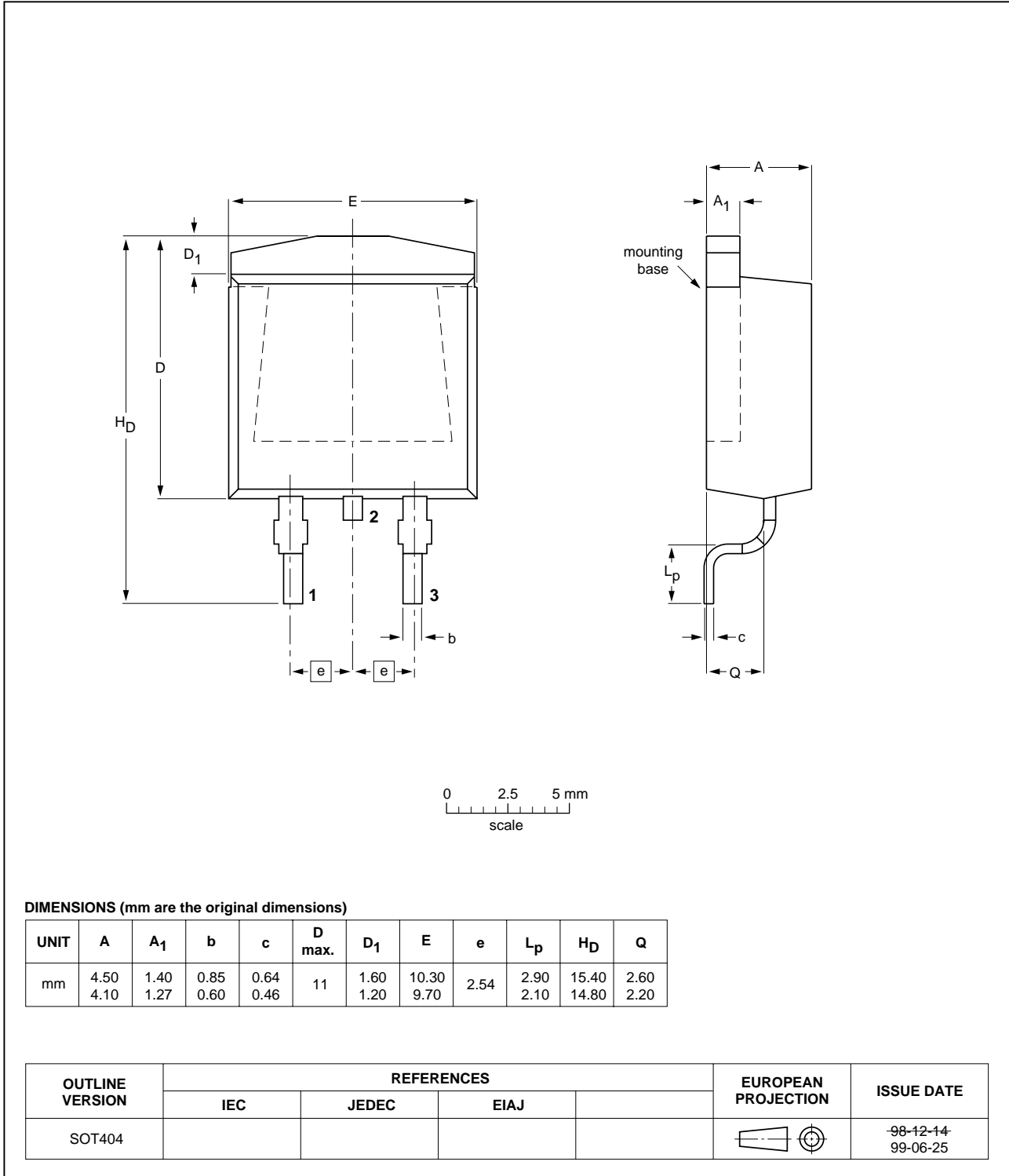


Fig 16. SO404 (D<sup>2</sup>-PAK).

## 10. Revision history

Table 6: Revision history

Rev	Date	CPCN	Description
01	20000907	-	Product specification; initial version.

## 11. Data sheet status

Datasheet status	Product status	Definition <sup>[1]</sup>
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued data sheet before initiating or completing a design.

## 12. Definitions

**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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